CLAIMS

We claim:

1.   A method for inserting delay in a timing path, comprising:

        determining a required delay between a driver and a receiver coupled to said driver;

        selecting a buffer to be coupled between said driver and said receiver to generate said required delay;

        determining an input transition time to said buffer from said driver;

        determining a desired effective load on said buffer that causes said buffer to generate said required delay under said input transition time;

        determining a desired effective length of a wire that generates said desired effective load;

        determining a length of a conductor between said driver and said receiver inside a bounding box that encloses said driver and said receiver;

        determining a maximum effective load generated by said length;

        if said desired effective load is less than or equal to said maximum effective load, selecting said buffer as a candidate to be inserted at a point inside said bounding box; and

        if said desired effective load is greater than said maximum effective load, selecting said buffer as a candidate to be inserted at a point outside said bounding box.

2.   The method of claim 1, wherein said determining an input transition time to said buffer comprises:

determining a location of a centroid of an output pin capacitance of said driver and an input pin capacitance of said receiver;

determining an effective load of a distance between said driver and said centroid;

determining an output transition time from said driver under said effective load and an input transition time to said driver;

determining a wire delay of said distance between said driver and said centroid; and

determining said input transition time to said buffer by adding said output transition time and said wire delay.

3.   The method of claim 1, wherein said determining a desired effective load comprises looking up said desired effective load from a cell-delay table for said buffer from said required delay and said input transition time.

4.   The method of claim 1, wherein said determining a desired effective load further comprises:

selecting another receiver coupled to said driver;

determining another effective load of said another receiver;

if said another effective load of said another receiver is less than said desired effective load of said receiver, flagging said another receiver to be coupled to said driver and reducing said desired effective load by said effective load of said another receiver.

5.   The method of claim 4, wherein said flagging occurs if:

a worst maximum path slack to said another receiver is greater than the required delay; and

the sum of said worst maximum path slack and a worst minimum path slack to said another receiver is greater than zero.

6.   The method of claim 1, wherein said selecting said buffer as a candidate to be inserted at a point inside said bounding box comprises:

selecting a point that is said desired effective length away from said receiver;

determining a length of a conductor between said driver and said selected point;

determining another input transition time to said buffer from said driver driving said length of a conductor between said driver and said point;

determining another desired effective load on said buffer that causes said buffer to generate said desired delay under said another input transition time;

determining an actual effective load on said buffer; and

selecting said buffer as a candidate to be inserted at said point between said driver and said receiver if said another desired effective load is greater than said actual effective load within a predetermined amount.

7.   The method of claim 6, wherein said determining another input transition time to said buffer comprises:

determining an effective load of a distance between said driver and said selected point; and

determining an output transition time from said driver under said effective load and an input transition time to said driver; and

determining a wire delay of said distance between said driver and said selected point; and

determining said another input transition time to said buffer by adding said output transition time and said wire delay. -

8. The method of claim 6, wherein said determining another desire effective load comprises looking up said another desired effective load from a cell-delay table for said buffer from said required delay and said another input transition time.

9. The method of claim 6, wherein said determining an actual effective load on said buffer comprises:

using a route model to estimate routing between said driver and said buffer and between said buffer and said receiver; and

determining said actual effective load from said routing.

10. The method of claim 6, further comprising selecting another point if said another desired effective load is not greater than said actual effective load by a predetermined amount, said selecting another point comprises:

performing a binary search on distances between said driver and said selected point if said another desired effective load is greater than said actual effective load by an amount greater than said predetermined amount; and

performing a binary search on distances between said selected point and said receiver if said another desired effective load is less than said actual effective load.

11. The method of claim 6, further comprising returning to said determining a length of a conductor between said driver and said selected point.

12. The method of claim 1, wherein said selecting said buffer as a candidate to be inserted at a point outside said bounding box comprises:

selecting a point on a Manhattan circle around said receiver, said Manhattan circle having a radius of said desired effective length;

determining a length of a conductor between said driver and said selected point;

determining another input transition time from said driver driving said length of a conductor between said driver and said selected point; and

determining another desired effective load on said buffer that generates said desired delay under said another input transition time.

13. The method of claim 12, wherein said determining another input transition time to said buffer comprises:

determining an effective load of a distance between said driver and said selected point; and

determining an output transition time from said driver under said effective load and an input transition time to said driver; and

determining a wire delay of said distance between said driver and said selected point; and

determining said another input transition time to said buffer by adding said output transition time and said wire delay.

14. The method of claim 12, wherein said determining another desire effective load comprises looking up said another desired effective load from a cell-delay table for said buffer from said required delay and said another input transition time.

15. The method of claim 12, further comprising:

determining an actual effective load on said buffer; and

selecting said buffer as a candidate to be inserted at a point outside said bounding box if said another desired effective load is greater than said actual effective load within a predetermined amount.

16. The method of claim 15, wherein said determining an actual effective load on said buffer comprises:

> using a route model to estimate routing between said driver and said buffer and between said buffer and said receiver; and

> determining said actual effective load from said routing.

17. The method of claim 15, further comprising selecting another point if said another desired effective load is not greater than said actual effective load within a predetermined amount, said selecting another point comprises performing a binary search on each edge of said Manhattan circle.

18. The method of claim 17, further comprising returning to determining a length of a conductor between said driver and said selected point.

19. The method of claim 1, wherein said selecting said buffer as a candidate to be inserted at a point outside said bounding box comprises:

> defining a first Manhattan circle around said receiver, said first Manhattan circle having a radius of said desired effective length;

> defining a second Manhattan circle around said driver, said Manhattan circle having a radius of a length of a conductor between said driver and said buffer that satisfies a maximum input transition time constraint; and

> if there is at least one point of intersection between said first and said second Manhattan circles, selecting said buffer as a candidate to be inserted at said one point between said driver and said receiver.

20. The method of claim 1, further comprising:

> selecting another buffer;

returning to said determining an input transition time to said buffer from said driver.

21. The method according to claim 20, further comprising performing a cost comparison to select one of said candidates, said cost comparison comprises:

determining a number of minimum path slacks that have become positive and a number of minimum path slacks that have become negative by each candidate through timing analysis;

determining a timing gain by each candidate through timing analysis;

if said number of fixed timing arcs of one of said candidates is greater than a best number of fixed timing arcs, adding said one candidate to a netlist;

if said number of fixed timing arcs is equal to said best number of fixed timing arcs and said number of worsened arcs is less than or equal to a best number of worsened arcs, adding said one candidate to a netlist; and

if said number of fixed timing arcs is equal to said best number of fixed timing arcs, said number of worsened arcs is greater than a best number of worsened arcs, and said gain is greater than a best gain, adding said one candidate to a netlist.

22. The method of claim 21, wherein said timing gain for each candidate is:

$$Gain = (scale * fPlus + fMinus) / dArea$$

wherein scale is a scale factor, fPlus is the increase in delay of all fixed arcs by a candidate, fMinus is the decrease in delay of all worsened arcs by a candidate, and dArea is the area of a candidate.

23. The method of claim 1, wherein said selecting a buffer comprises:

sorting a plurality of buffers by the ascending order of their delays at an effective load of all elements coupled to said driver, and at an input transition time to said receiver from said driver with said effective load on said driver; and

selecting one of said buffers with the smallest delay.

24. A method for selecting nodes to be optimized, comprising putting nodes into a plurality of criticality bins, wherein each criticality bin stores nodes with a corresponding range of minimum path slacks and a corresponding range of maximum path slacks.

25. The method of claim 24, wherein said plurality of criticality bins comprises:

a first criticality bin for nodes with critical minimum path slacks and non-critical maximum path slacks;

a second criticality bin for nodes with sub-critical minimum path slacks and non-critical maximum path slacks

a third criticality bin for nodes with critical minimum path slacks and sub-critical maximum path slacks;

a fourth criticality bin for nodes with sub-critical minimum path slacks and sub-critical maximum path slacks;

a fifth criticality bin for nodes with critical minimum path slacks and critical maximum path slacks; and

a sixth criticality bin for nodes with sub-critical minimum path slacks and critical maximum path slacks.

26. The method of claim 25, wherein:

said critical minimum path slacks include minimum path slacks less than a first minimum slack;

said sub-critical minimum path slacks include minimum path slacks greater than said first minimum slack and less than a second minimum slack;

said non-critical minimum path slacks include minimum path slacks greater than said second minimum slack;

said critical maximum path slacks include maximum path slacks less than a first maximum slack;

said sub-critical maximum path slacks include maximum path slacks greater than said first maximum slack and less than a second maximum slack; and

said non-critical maximum path slacks include maximum slacks greater than said second maximum slack.

27. The method of claim 26, wherein:

the first minimum slack is 0;

the second minimum slack is 100 picoseconds;

the first maximum slack is 0; and

the second minimum slack is 100 picoseconds.

28. The method of claim 24, further comprising:

selecting a criticality bin from said plurality of criticality bins; and

` putting nodes in said selected criticality bin into a number of a plurality of slack bins divided between a first minimum path slack and a second minimum path slack.

29. The method of claim 28, wherein the first minimum path slack is the most negative minimum path slack of the nodes in said criticality bin and the second minimum path slack is 0.

30. The method of claim 28, further comprising:

selecting a slack bin from said plurality of slack bins; and

putting nodes in said selected slack bin into a plurality of level bins according to their node levels in timing paths.

31. The method of claim 30, further comprising:

selecting a node; and

optimizing said node to remove a timing violation.

32. The method of claim 31, wherein said optimizing said node comprises:

determining a required delay between a driver and a receiver;

selecting a buffer to be inserted between said driver and said receiver;

determining an input transition time to said buffer from said driver;

determining a desired effective load on said buffer that causes said buffer to generate said required delay under said input transition time;

determining a desired effective length of a wire that generates said desired effective load;

determining a length of a conductor between said driver and said receiver inside a bounding box that encloses said driver and said receiver;

determining a maximum effective load generated by said length of a conductor;

if said desired effective load is less than or equal to said maximum effective load, inserting said buffer at a point inside said bounding box; and

if said desired effective load is greater than said maximum effective load, inserting said buffer at a point outside said bounding box.

33.   The method of claim 31, further comprising:

    performing an incremental analysis to re-determine minimum and maximum path slacks of nodes affected by said optimization; and

    again putting said nodes in said plurality of level bins according to their node levels in timing paths.

34.   The method of claim 33, further comprising:

    reducing said the number of a plurality of slack bins by one;

    again putting said nodes in said plurality of slack bins.

35.   The method of claim 34, further comprising again putting said nodes in said plurality of criticality bins.